A1

3. (Amended) The phase lock loop according to claim 8, further comprising a loop filter coupled between the phase/frequency detector and the timing reference generator, the loop filter developing a control voltage for the timing reference generator.

A2 SUB C1

8. (Amended) A phase lock loop comprising:

a detector for comparing a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal;

a timing reference signal generator, connected in feedback fashion to provide a timing reference signal to the detector, the timing reference signal generator being operatively configured to produce an output signal at a characteristic frequency an integral multiple of a desired output clock frequency and to produce an output signal at a characteristic frequency M times the frequency of a desired output clock frequency and being constructed to output multi-phase signals, each phase signal oscillating at the characteristic frequency, wherein the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency;

a frequency divider circuit coupled to receive the output signal and reduce its characteristic frequency to a desired output clock frequency; and

a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, the phase select MUX being a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

9. (Unchanged) The phase lock loop according to claim 8, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

10. (Unchanged) The phase lock loop according to claim 9, wherein the frequency divider circuit is constructed of current mode logic components.

11. (Unchanged) The phase lock loop according to claim 9, wherein the phase control MUX is constructed of current mode logic components.

19. (Amended) The timing circuit according to claim 21, wherein the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency.

21. (Amended) A feedback controlled timing circuit, comprising:

a comparison circuit configured to compare a frequency characteristic of an input signal to a frequency characteristic of a timing reference signal, the comparison circuit asserting control signals in response to said comparison;

a timing reference signal generator, connected to provide a timing reference signal to the comparison circuit, the timing reference signal generator responsive, in feedback fashion, to said control signals asserted by the comparison circuit, the timing reference signal generator being configured to develop an output signal at a frequency M times the frequency of a desired output clock signal, the desired output clock signal having a frequency characteristic N times the frequency characteristic of the input signal, the timing reference signal generator being implemented as a